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Research Article

Modelling and Simulation of Hetero-Dielectric Junction-less TFET for Low Power Applications

Sagarika Choudhury* and Krishna Lal Baishnab

Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam, 788010, India

***Corresponding Author:** Sagarika Choudhury, Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam, 788010, India.

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Abstract

This paper put forwards afresh concept to improvise the conventional JL-TFET. The choice and placement of dielectric are crucial in determining the efficiency of the device. Thus, asymmetric hetero-dielectric is found to improve the gate control and also aid in lowering capacitance. The concept of triple gate material has been incorporated which resulted in better gate control and thereby improving ON-current. The proposed structure reports a current ratio of 4.4 x10^{10}A and promising values for Subthreshold Swing (SS) 9 mV/dec (point) and 48 mV/dec (average).This improvised structure helps in development of devices suitable for low power applications. The simulation based study was performed in July 2021 and compared with the results available.

Keywords: TFET; JLTFET; Hetero-dielectric; Asymmetry

Introduction

The growth of semiconductor industry has increased many fold in recent decade. Researchers are coming up with many new ideas to outperform the demerits of conventional devices and improve their efficiency. With the ongoing miniaturisation and improvisation, the Junction less devices [1] came into picture to overcome the difficulty of fabricating [2-4] abrupt junctions [5]. Moreover, in recent times TFET [6, 7] is one major replacements for conventional devices specifically for low power applications. JLTFET is basically an amalgamation of two concepts: JLFET with tunnelling phenomenon. It works on the principle of work function modulation [1] wherein a uniformly doped n-type device is made to behave as PIN structure. Moreover, this work also tries to incorporate the advantage of TMG [8-10] for better gate control along with asymmetry for improved performance. With the use of high k near tunnelling junction the electric field [11] across the junction increases, and this in turn increases the tunnelling efficiency, thus ON-current is increased. Similarly, the use of low k near drain resulted in decrease in OFF- current. Hence, it has been observed that the use of TMG with asymmetric hetero-dielectric significantly enhances the current ratio with moderate values for SS. A numerous number of analytical models for junction less TFETs are discussed in various literature [1, 12, and 13]. The simulations are carried out in TCAD simulation tool.

This work has the following sections: starts with describing the device structure, subsequently results are discussed and finally the conclusion section is presented.

Device Structure

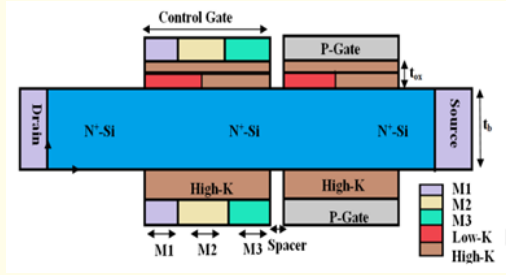

Figure 1: AHD-TMG-JLTFET structure.

An Asymmetric Hetero-dielectric Triple Material Gate Junction less TFET is proposed. This structure overcomes the drawback of conventional JLTFET by improving the ON- current. Fabricating abrupt junction is quite difficult [12], thus, junction less structures with uniform doping across the device comes to the limelight. The structure is designed on silicon base with uniform doping of $1x10^{19}$ cm^{-3}. Moreover, due to incorporation hetero-dielectric in asymmetric technique, low-k material is added across the drain. This in turn results in low capacitance. The asymmetry in the structure improves the gate control capacity. Improved ON-current and low capacitance are the key factors that makes a device ideal for low power applications. Two gates are incorporated in the proposed structure: Polar gate at zero bias for inducing P region and Control gate for inducing channel region by work function variability. The control gate has three metal [14] with different work-function. Each section is labelled as M1, M2, and M3 with length L1, L2 and L3. Synopsis TCAD tool is used to perform all the simulations. The length and other dimensions are listed in table 1.

Parameters	***Values***
L1	6nm
L2	12nm
L3	6nm
t_{oxf}	3nm
t_b	3nm

Table 1: Dimension of device.

Results and discussion

Device Characteristics

Figure 2 portrays the study of work function variability of control gate. An On-current of 4.4×10^{-4} A and OFF-current of 1×10^{-14} A for control gate work function of 4.7 eV and polar gate work function of 5.93eV is found. However, the Polar gate work function significantly impacts the polarization charge in the source region. With increase in the work function the bands move up, effective tunnel width increases in the tunnel junction, thereby, it increases ON current while keeping OFF current in permissible limit. Thus, Polar work function of 5.93 eV modulates the carrier density below the gate and helps in achieving the best current ratio as depicted in fig 3.

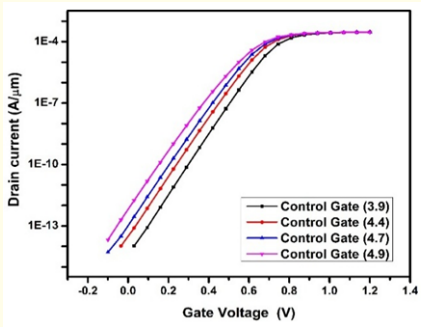

Figure 2: I_D -V_{GS} for varies workfunction (Control gate).

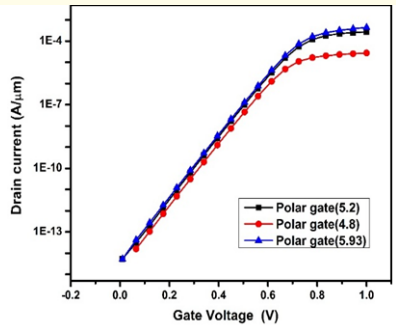

Figure 3: I_D -V_{GS} plot for different work function.

Moreover, physical renovation also resulted in improved SS average. The values obtained for Subthreshold Swing (SS) are 9 mV/dec (Point) and 48 mV/dec (Average). The average SS is calculated by calculating minimum and threshold voltages. Thus, to calculate the threshold voltage the current is kept constant. At a constant current of $1x10^8$A/μm, the threshold voltage of 0.34 is obtained. The leakage current and SS value also reflects much improvement. The analog performance depends substantially on the transconductance of the device defined by the formula stated in equation (1). Fig.4, reports the g_m of the AHD-TMG-JLTEFT as 1×10^{-3} S/μm and it is reasonably greater than reported JLTFET's.

$$g_m = \frac{dI_D}{dV_{gs}} \qquad (1)$$

The gap between the gates is another important parameters impacting the fringe field effect in the device. Increasing the gap between the gates increases the OFF-current. Fig 5 shows that a gap of 1nm gives the best current ratio.

The gate dielectric also modulates the device performance. Symmetric dielectric (SiO_2) has much higher OFF-current as shown in fig 6. An asymmetric hetero-dielectric provides the best current ratio.

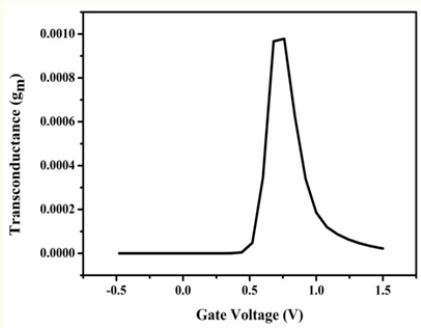

Figure 4: Transconductance Plot.

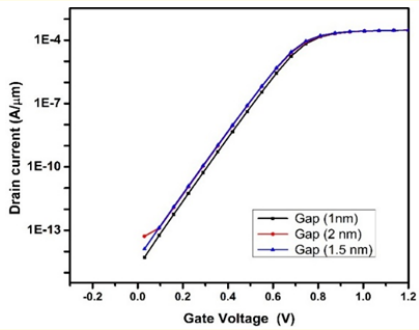

Figure 5: I_D -V_{GS} as function gap between gates.

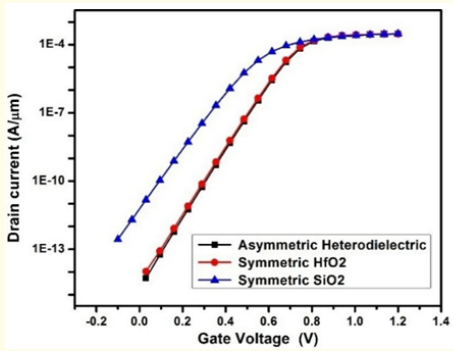

Figure 6: I_D -V_{GS} as function of gate dielectrics.

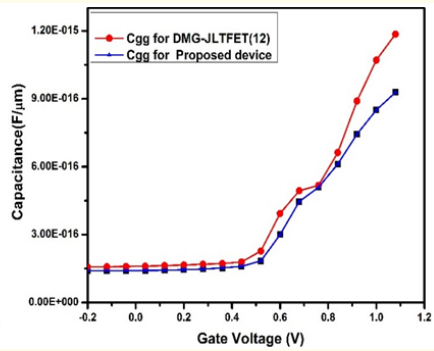

Figure 7: Capacitance comparison with existing structure.

I_{ON} (A/μm)	I_{OFF} (A/μm)	Ratio	V_{th} (V)	SS (Average)	SS (Point)	References
$36x10^{-6}$	$5x10^{-14}$	$6x10^{8}$	0.4	70	38	Ref [1]
$18x10^{-5}$	$3x10^{-13}$	$6x10^{8}$	0.4	-	17	Ref [12]
$1x10^{-6}$	$1x10^{-13}$	$6x10^{7}$	0.8	48	-	Ref [14]
4.4×10^{-4}	1×10^{-14}	4.4×10^{10}	0.34	48	9	Proposed work

Table 2: Showing the comparison with reference works.

The table 2 portrays the comparison amongst various junction less devices proposed in the literature. The structure shows massive improvement in SS values along with current ratio proving the utility of the device. The capacitances are computed at a frequency of 1MHz. Due to usage of asymmetric dielectric the total gate capacitance of TMG-AHD JLTEFET is lower compared to conventional DMG-JLTFET [15]. Again, a plot depicting comparison amongst various junction less structures in terms of surface potential is shown in fig.8. The surface potential is a significant device parameter for analysing device performance. Since, with increase in surface potential the electric field also improvises at the junction, thereby increasing tunnel efficiency. The step profile of surface potential is as a result of the use of three different gate material. It has been observed that the rate of variation is slightly elevated across drain junction due to certain assumptions made while developing the model. Furthermore, the comparison with conventional JLTFET is shown in fig. 9.

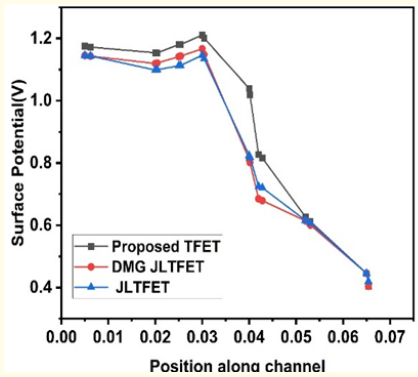

Figure 8: Surface Potential of various structures.

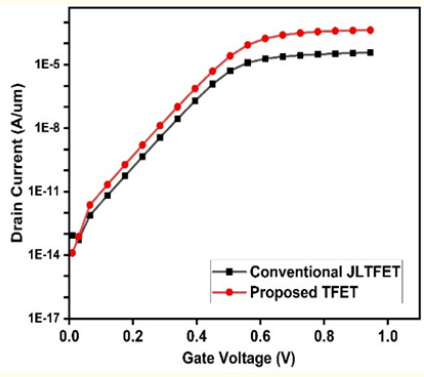

Figure 9: I_D -V_{GS} as function of gate voltage at Vds = 1V, Vgs = 1V.

Conclusion

A detailed study of the proposed structure is performed by analytical modelling and simulating the device in TCAD software. It is observed that the performance of this conventional JLTFET can be improvised by using asymmetric combination of high k and low k dielectric. The performance of the proposed device is found to be suitable for low power applications. Moreover the performance achieved is compared with the existing structure present in the literature. It has been observed that the proposed structure shows improvement in current ratio as well as SS which makes it an adroit candidate for low power application. Thus, this Si based device reports an improved ON-current of 4.4×10^{-4} A, OFF current of 1×10^{-14} A. and current ratio of 4.4×10^{10} and SS value 9 mV/dec (point) and 48 mV/dec (average).

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